Name:

Registration Number:

1. Consider an nMOS transistor in a 0.6 μm process with W/L = 4/2 λ (i.e., 1.2/0.6μm). In this process, the gate oxide thickness is 100 Å and the mobility of electrons is **DOB** cm^2/V· s. The threshold voltage is 0.7 V.

a. Plot Ids vs. Vds for Vgs = 0.7v and **ID** for NMOS ONLY. 3+3

**ID** = (Your Registration Number % 4)+1

**DOB =** (Your date of birth in DDMMYYYY % 100)+10

Example: 19201071 was born on 17th August 2001 have

Will have ID = (19201071 % 4)+1 = 4

DOB = (17082001%10) +10= 11

b. Show only Beta calculation for PMOS. 4